ABSTRACT

A pipelined, simultaneous and redundantly threaded ("SRT") processor configured to detect transient faults during program execution by executing instructions in at least two redundant copies of a program thread and wherein misspeculation caused by incorrectly predicting the outcomes of branch instructions in a second program thread is avoided by using the actual outcomes of branch instructions in a first program thread to correctly predict the outcome of branch instructions in the second program thread. The SRT processor comprises a branch predictor for speculating the outcomes of branch instructions in the first program thread and a branch outcome queue for storing the actual outcomes of branch instructions in the first program thread. The processor uses the branch outcome queue and not the branch predictor to predict the outcomes of branch instructions in the second program thread.